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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/798,890
Filing Date: March 12, 2004
Appellant(s): BURDASS, ANDREW

Stanley C. Spooner
Reg. No. 27,393
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08 June 2007 appealing from the Office action mailed 27 November 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claim Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Nguyen, U.S. Patent No. 5,481,685

Glass, U.S. Patent No. 5,784,602

Birk, U.S. Patent No. 6,978,350

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-12 and 24-27 are rejected under 35 U.S.C. 102(a) and (e) as being anticipated by Birk (U.S. Patent No. 6,978,350).

Regarding claims 9 an d 24, Birk discloses apparatus for processing data, said apparatus comprising: a cache memory (fig. 2 reference 12) operable to store program instructions to be executed (col 2 lines 29-30); an instruction pipeline including an instruction prefetch unit (col 2 lines 42-45) and an exception controller responsive to an exception signal to trigger exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location (col 2 lines 58-61);

wherein upon receipt of said exception signal part way through execution of a current program instruction, said exception controller is operable to trigger a lookup of said exception handling program instruction within said cache memory (col 2 lines 35-

49) and if said exception handling program instruction is not present within said cache memory to trigger a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory (col 2 lines 47-50).

And upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory (col 2 lines 36-49).

3. Regarding claims 10 and 25, Birk discloses apparatus as in claim 9, wherein execution of said current instruction lasts for a plurality of clock cycles and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles (col 3 lines 16-22).

4. Regarding claims 11 and 26, Birk discloses apparatus as in claim 9, wherein said exception handling program instruction redirects program execution to an exception handling routine (col 2 lines 58-61).

5. Regarding claims 12 and 27, Birk discloses apparatus as in claim 9, wherein said exception controller is an interrupt controller, said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction (col 2 lines 58-61).

Claim Rejections - 35 USC § 103

6. Claims 13 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birk in view of Nguyen (U.S. Patent No. 5,481,685).

7. Regarding claims 13 and 28, Birk discloses apparatus as in claim 9.

Birk fails to disclose an exception that complete a data abort or a prefetch abort.

Nguyen discloses a data abort (col 14 line 62 o col 15 line 4) and a prefetch abort (col 27 line 2-5).

Examiner asserts that the functionality described in Nguyen is very common for processing systems. The motivation for this functionality is twofold: 1) the processing system is required to process the ISP instructions, so it must halt production on remaining instructions; 2) interrupts can change the flow of program execution, so the instructions are aborted so that unnecessary calculations are not made.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Birk and allow it to utilize the data and prefetch abort as disclosed in Nguyen.

8. Claims 14, 15, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birk in view of Glass (U.S. Patent No. 5,784,602).

Regarding claims 14, 15, 29 and 30, Birk discloses the limitations of claims on which these claims are dependent.

Birk fails to disclose a common core for processor components or, more generally, an integrated circuit.

Glass discloses a system on an integrated circuit (col 4 lines 21-25).

At the time of the invention, one skilled in the art would have been motivation to make the combination based on the reasoning disclosed in Glass that an integrated circuit "is highly advantageous for space, speed, power consumption and cost reasons" (col 4 lines 23-25).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Birk and implement it on a single integrated core, as in Glass.

(10) Response to Arguments

A. Appellant argues whether "upon completion of execution of said current program instruction..." is disclosed in Birk.

Appellant state:

"Appellant's independent claims 9 and 24 both specify the conditional phrase that, upon "completion of execution of said current program instruction" certain other specified actions take place ("upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory." See Claims 9 and 24) The Examiner alleges that this conditional phrase is disclosed in Birk at Col. 2, lines 36-49. However, a review of these lines indicates that there is no such conditional phrase disclosed in the Birk reference. In fact the cited portion of Birk says nothing about any aspect of "upon completion of execution of said current program" The Examiner fails to disclose where this claimed conditional interrelationship between claimed elements is taught in Birk. In fact, he apparently fails to appreciate the Birk actually teaches the direct opposite of this claim requirement. Birk at column 3, lines 59-63, states that "since the DSP 10 aborts the instructions in the pipeline upon detection of an interrupt, it aborts the instruction which generated the cache line miss and begins execution of the interrupt service routine." (emphasis added). Accordingly, the instruction in Birk is not completed (contrary to the claimed requirement of "upon completion"), and this failure to complete is necessary for the proper operation of the Birk reference. Birk does not explain how it is able to tolerate aborting such a partially completed instruction.

The limitation Appellant argues is as follows: "upon completion of execution of said current program instruction, if said exception is still current, then said instruction

prefetch unit fetches said exception handling program instruction from said cache memory."

1. First part: "upon completion of execution of said current instruction"

Separating this limitation, the first portion is "upon completion of execution of said current program instruction." Appellant argues that this limitation requires completion of the current program instruction; however, even if this is the case, Birk meets this requirement.

As Appellant correctly points out, Birk col. 3 lines 59-63 discloses that when an exception occurs, the pipeline is flushed, hence aborting the instruction. Appellant's argument is, essentially, that the claim limitation is not met because Birk does not complete the instruction. This contention is incorrect.

As one of ordinary skill in the art is well aware, a computer program contains a list of instructions that must be completed in the correct order (with respect to retirement) for the program to function correctly. To suggest that an instruction is never completed is completely contrary to the teachings of Birk and the knowledge of one of ordinary skill in the art of instruction processing. The aborted instruction must be reissued and, therefore, is completed as required by the claim.

This is also supported by Birk col 4 lines 5-6: When the ISR has run to completion, execution returns to the lower priority task which generated the cache miss."

2. Second part: "if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory."

Looking at the second part of the limitation, Birk must be evaluated at the time the aborted instruction is reissued and completed. Col 3 line 57 to col 4 line 7 shows Birk's disclosure of the exception handling routine (aka interrupt service routine). Birk makes it clear that during execution of an instruction, an interrupt occurs. The pipeline (including the interrupted instruction) is aborted and the exception handler is run. Upon completion of the exception handler, the "lower priority task which generated the cache miss" is resumed, indicating that the aborted instruction is reissued.

Putting this limitation in its complete context, it is appropriate to determine the following: upon completion of the aborted instruction (meaning, when it was reissued and completed) will the exception still be current? The answer will always be "no"; the exception handler has already run its course.

Therefore, the "if" limitation of the claim is never met by Birk, meaning that the following limitation ("said instruction prefetch unit fetches said exception handling program instruction from said cache memory") is never required by the disclosure of Birk at the time of the aborted instruction's completion.

B. Applicant argues Examiner's assertion on page 3

Appellant argues that examples assertion, "[n]ote that the instruction service routine comprises a plurality of instructions. So it follows the memory hierarchy outlined in col 2 lines 36-49."

Examiner acknowledges that this comment, in context of the rejection is confusing. Examiner has withdrawn the comment in the current rejection. The withdrawal of this side note does not affect the applicability of the current rejection. It is also noted that Appellant's argument with respect to this comment does not assert that the rejection of any claim limitations hinges on the substance of the comment.

C. Appellant argues the rejection of the "if...,then..." condition.

Appellant states:

"The Examiner construes the "if..., then..." element interrelationship of claims 9 and 24 to be met if, as he argues in the Final Rejection, page 3, lines 12- 14, the Birk teaching discloses that the behavior takes place both if the exception is still current and if the exception is not still current. This is believed to be an improper interpretation of this portion of Appellant's claim. The claim language positively recites "upon completion of execution of said current program instruction, if said exception is still current~ then said instruction prefetch unit fetches .... " The Examiner has provided no support for his misinterpretation of the claim language which clearly states that "if said exception is still current, then said instruction prefetch unit fetches." Not only has the Examiner misinterpreted the claim language, but he has failed to identify where there is any equivalent teaching in Birk. There is certainly no identification that an exception controller having the claimed interrelationship is disclosed in the Birk reference. It should also be noted that nowhere in the Final Rejection does the Examiner allege any other prior art reference of record to disclose the "if..., then..." interrelationship which is clearly missing from Birk. Thus no reference of record discloses this claimed feature."

The current interpretation of the claims with respect to this limitation is discussed above in (A). Examiner hopes that this addresses Appellant's concerns with respect to lack of support from Birk.

Appellant further appears to argue that the "if...then..." statement requires an occurrence of the limitation disclosed after the "if" portion. This is incorrect. As an example, consider the phrase, "If John goes to the store today, then he will purchase bread." Then, in actuality, John chooses not to go to the store. The "if...then..." statement above is not rendered incorrect by the actions of John. The statement is still

true. The reason for this, of course, is because the "if...then..." statement in no way requires an occurrence of the "if" portion.

Consequently, as a reiteration of the point discussed in (A) it is not required that "upon completion of execution of said current instruction" that the exception will ever be current; in fact, in Birk, it never is.

D. Appellant argues the motivation for combining Birk and the secondary references. In particular, Appellant argues the combination with respect to Glass.

Appellant states:

"the Examiner's statement that one skilled in the art would have been motivated to make the combination based on the reasoning disclosed in Glass (i.e., that an integrated circuit is 'highly advantageous for space, speed, power consumption and cost reasons" (Glass, column 4, lines 23-35)) does not provide any reason or motivation."

It is completely unclear to Examiner why Appellant does not believe that saving on space, speed, power and cost would be adequate motivation for one of ordinary skill in the art. Appellant further argues that there is no indication in the primary reference that such features would be advantageous.

Little detail is necessary to explain why the elements above are clearly an advantage for any processing system; this is simply common sense. Birk explicitly discloses that it desires to "improv[e] the throughput of cache-based embedded processors (col 1 lines 51-52). With this in mind, it is unclear why Appellant does not believe that an increase in speed (as Glass indicates would occur with an integrated circuit) would not be advantageous to Birk.

In reality, most every modern processing system is placed in an integrated circuit; Birk was more than likely intended to be created on such a circuit. Even the disclosure of Birk gives a strong indication of this: "A processor such as a digital signal processor (DSP) 10 and a cache memory 12 are located on a single processing chip 14." (col 2 lines 26-28). Perhaps this disclosure alone is enough for an anticipatory rejection with respect to an integrated circuit; however, Examiner determined that this statement was not completely adequate for such a rejection. Therefore, an obvious rejection was made. Arguing against the validity of an obvious-type rejection in view of Glass, however, is completely contrary to both common art and common sense.

E. Appellant argues that Birk teaches away from the claimed combination.

Appellant states:

"As noted above, Birk teaches the abortion nof the instruction which generated the cache line miss and thus the instruction is not completed. As noted, this is the direct opposite of Appellant's claim requirement "upon completion of execution of said current program instruction." (emphasis added. Thus, Birk, in teaching the direct opposite of Appellant's claimed exception controller, would tend to lead one of ordinary skill in the art away from Appellant's invention."

Appellant further states:

"Moreover, the Examiner has failed to explain how or why one of ordinary skill in the art would ignore this contrary teaching of Birk when attempting to make the combination of Birk with either Nguyen or Glass in the rejections of claims 13-15 and 28-30. As a consequence, neither of these combinations would be obvious in view of the Birk reference."

Appellant's argument is somewhat unclear. Appellant states that the argument is regarding an obvious type rejection, but simply repeats the argument of the anticipatory rejection discussed in (A) and (C). Appellant's argument appears to be that since

Examiner does not disclose a limitation of the independent claim, this teaches away from the combination of secondary references.

Examiner does not see why this is the case. Even if Appellant's assertion were true regarding the improper anticipatory rejection (which, as shown in (A) and (C) above, it is not) it does not follow that the combinations with Nguyen and Glass are improper. Nguyen was added because Birk fails to disclose a data abort and prefetch abort instruction. Glass was added for the disclosure of an integrated circuit. These additions have nothing to do with "aborted instruction" discussed above; therefore, Birk does not teach away from these combinations.

F. Appellant argues the anticipatory rejection of the "if...,then...." statement

Appellant's argument appears to simply be a reiteration of the arguments presented above, but in less detail. Appellant's attention is directed to sections (A) and (C) above.

G. Appellant argues the obviousness rejection with respect to Birk and Nguyen

1. Appellant argues that, since the anticipatory rejection is improper, the obvious rejection is also improper.

Examiner disagrees. The anticipatory rejection is entirely appropriate. See (A) and (C) above.

2. Appellant argues that there is no motivation for combination.

Examiner disagrees. Appellant appears to ignore the final paragraph in page 4 of the Final Office Action mailed on 27 November 2006:

"Examiner asserts that the functionality described in Nguyen is very common for processing systems. The motivation for this functionality is twofold: 1) the processing system is required to process the ISP instructions, so it must halt production on the remaining instructions; 2) interrupts can change the flow of program execution, so the instructions are aborted so that unnecessary calculations are not made."

3. Appellant argues that Birk teaches away from the claimed invention.

Appellant reiterates the arguments of section (E) which, in turn, are a reiteration of the arguments of sections (A) and (C). Accordingly, Appellants attention is directed to sections (A) and (C) for the appropriate response.

H. Appellant argues the combination of Birk and Glass

Appellant's argument appears to be a summary of arguments made or reiterated elsewhere in the Appeal Brief. No specific limitations are traversed and no specific arguments are made exception for the motivation of the Birk/Glass combination. This is discussed in section (D) above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

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07 December 2006

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